## Introduction

The DS2761 High-Precision Battery Monitor provides monitoring and protection for a Li+ cell. When the device powers up, the state of the DQ pin, the Power Mode bit (PMOD) and the battery voltage can affect what mode the device enters and how the Charge Control (CC) and Discharge Control (DC) pins react. This Application Note will provide details of what happens in many possible powering up scenarios.

## Powering Up a DS2761

When the DS2761 goes through its power on reset (POR) sequence, the device begins in Sleep Mode until a condition that brings the device into Active Mode is encountered.

In the following powering up cases of the DS2761, all device EEPROM is recalled to the shadow RAM during the POR sequence. At power up, the Accumulated Current Register (ACR) is reset to 0.00mAhrs and the User RAM is undefined.

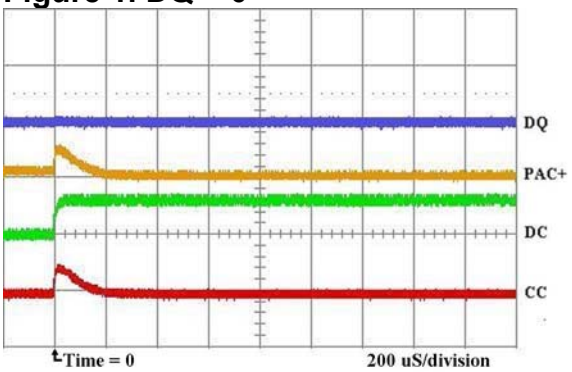
The following table contains the conditions at power up that will be examined in this Application Note.

| CASE | POWER UP CONDITIONS | | | |
|---|---|---|---|---|
| | PMOD | SWEN | DQ | $V_{IN}$ |
| A | -- | -- | 0 | -- |
| B | 0 | -- | 1 | -- |
| C | 1 | -- | 1 | > $V_{UV}$ |
| D | 1 | -- | 1 | < $V_{UV}$ |

### Case A: DQ = 0

If DQ is low when power is first applied to a DS2761, the device stays in Sleep Mode. The DC pin is pulled to the cell voltage, which disables the PAC+ terminal. The PAC+ terminal is pulled low when the device is in Sleep Mode. The CC pin is pulled to PAC+, so that CC is low, but the charge FET remains disabled. When DQ is low, the state of PMOD has no effect on the control pins because the device will not wake up in either case. The waveform in this case is also independent of the cell's voltage in relation to the under voltage threshold ($V_{UV}$).

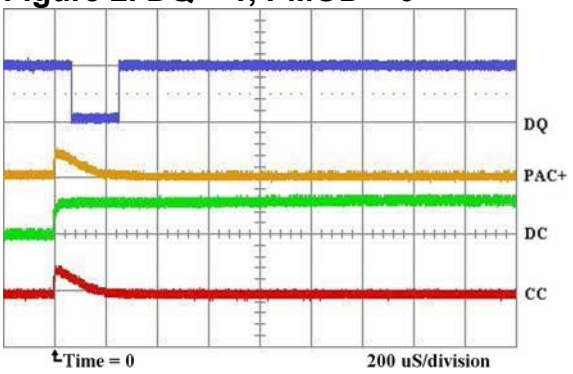
**Figure 1. DQ = 0**



## Case B: DQ = 1, PMOD = 0

If DQ is high and PMOD is 0 at power up, the DS2761 will pull the DQ line low as if it were responding to a 1-Wire® Reset. The other pins exhibit the same result as if DQ were low because the device remains in Sleep Mode and PAC+ does not become active. The waveform in this case is also independent of the cell's voltage in relation to $V_{UV}$.

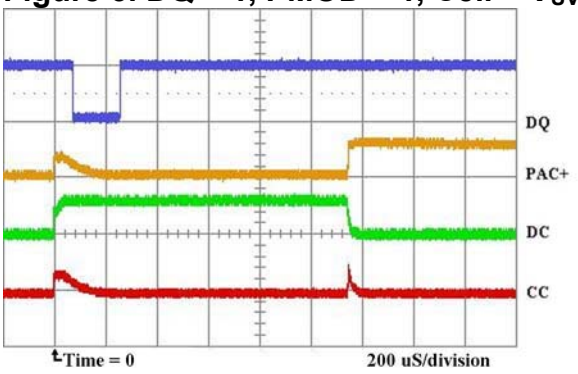
**Figure 2. DQ = 1, PMOD = 0**




## Case C: DQ = 1, PMOD = 1, Cell > $V_{UV}$

If PMOD is 1, the DS2761 does power up into Active Mode if DQ is also high. DQ is pulled low as the DS2761 responds with a presence detect as power is applied to the device. For the first 1ms, the DC pin is pulled to the cell voltage, which disables PAC+ and the CC pin is pulled to PAC+, so that CC is low, but the charge FET remains disabled. The PAC+ terminal remains disabled for approximately 1ms until both CC and DC are driven low.

**Figure 3. DQ = 1, PMOD = 1, Cell > $V_{UV}$**

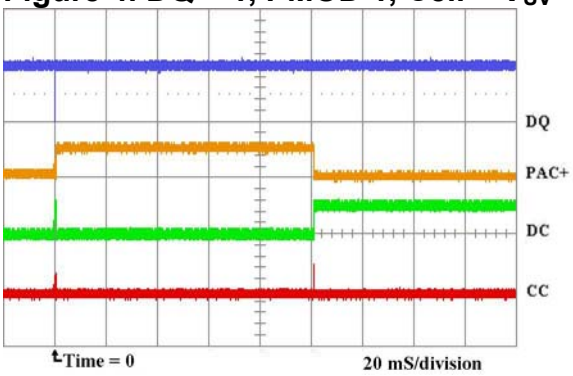



*1-Wire is a registered trademark of Dallas Semiconductor.*

### Case D: DQ = 1, PMOD 1, Cell < $V_{UV}$

If the cell voltage is below $V_{UV}$ when the same scenario as Case C occurs, the waveforms are identical for the first 100ms. However, after 100ms, the under voltage condition is detected and the device goes into Sleep Mode and PAC+ is disabled as the DC pin is pulled to the cell voltage. The CC pin is driven low for the first 100ms and then as the device enters Sleep Mode, the CC pin is pulled to PAC+ so that it remains low, but the charge FET is now disabled.

**Figure 4. DQ = 1, PMOD 1, Cell < $V_{UV}$**




## Summary

The state of the protection pins at the time that power is applied to the DS2761 depends on the settings of the PMOD bit, the DQ line and the cell voltage. This is important when designing circuits and software to recover from an event that causes the device to temporarily lose power. This Application Note also applies to the C2 Revision of the DS2760.